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(71) Applicant: **Alcatel N.V.**
Strawinskylaan 537
NL-1077 XX Amsterdam(NL)
Applicant: **BELL TELEPHONE
MANUFACTURING COMPANY Naamloze
Vennootschap**
Francis Wellesplein 1
B-2018 Antwerp(BE)

(72) Inventor: **Vermeulen, Christophe Daniel**

Ghislain
36 Rue de Watrelos
B-7520 Ramegnies-Chin(BE)
Inventor: **van der Putten, Frank Octaaf**
oude Wichelsesteenweg 25
B-9340 Lede(BE)
Inventor: **Voeten, Bart Frans**
Gasthuisstraat 6
B-2340 Beerse(BE)

(74) Representative: **Vermeersch, Robert et al**
**BELL TELEPHONE MANUFACTURING
COMPANY Naamloze Vennootschap Patent
Department Francis Wellesplein 1**
B-2018 Antwerpen (BE)

(54) **Video decoder.**

(57) A video decoder is proposed which receives packets of video information relating to moving video images from a packet switching network. In accordance with the invention a lot of hardware overhead is eliminated and much flexibility gained compared to prior art decoders in letting the decoding process, implemented via a decoding means (DEC1, DEC2), run asynchronously with respect to the display process, implemented via a display means (DIS). Moreover, and also in contrast with prior art decoders, the video decoder according to the present invention is not explicitly synchronized to its corresponding encoder by explicitly recovering the latters system clock. This is realized through buffering actions within a frame store memory (FSM) placed between the decoding means (DEC1, DEC2) and the display means (DIS). The variable length of such a buffer can be used to control the speed of the display process in order to prevent underflow or overflow of the latter buffer and corresponding image degradation. The latter is done via a control means (CON).
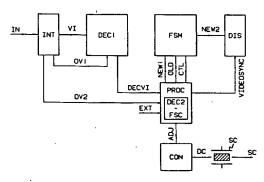
FIG.1